

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board

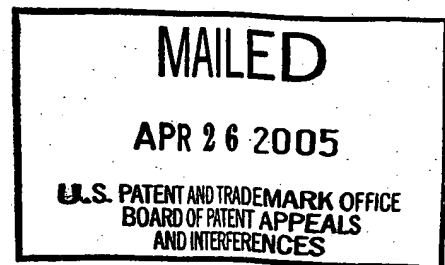
UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte AFTAB AHMAD

Appeal No. 2005-0426
Application No. 09/397,952

ON BRIEF



Before HAIRSTON, GROSS, and BARRY, Administrative Patent Judges.
HAIRSTON, Administrative Patent Judge.

DECISION ON APPEAL

This is an appeal from the final rejection of claims 1, 3, 5, 7 through 15, 23 and 25 through 28.

Appeal No. 2005-0426
Application No. 09/397,952

The disclosed invention relates to a process for forming a gate structure on a semiconductor substrate that comprises the steps of implanting nitrogen into the substrate, and conducting a source/drain reoxidation of the substrate to thereby form a nitride layer.

Claim 1 is illustrative of the claimed invention, and it reads as follows:

1. A process of forming a gate structure on a semiconductor substrate, comprising:

providing a semiconductor substrate having a channel region formed therein so as to define a source and a drain region and a gate structure comprised of a gate dielectric positioned on said channel region and a conductive layer positioned on said gate dielectric;

implanting nitrogen into said substrate; and

conducting a source/drain reoxidation, thereby forming a sidewall spacer after implanting said nitrogen.

The references relied on by the examiner are:

Ahmad et al. (Ahmad)	5,405,791	Apr. 11, 1995
Arai et al. (Arai)	5,972,783	Oct. 26, 1999 (filed Feb. 6, 1997)

Claims 1, 3, 5, 7 through 15, 23 and 25 through 28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ahmad in view of Arai.

Appeal No. 2005-0426
Application No. 09/397,952

Reference is made to the briefs and the answer for the respective positions of the appellant and the examiner.

OPINION

We have carefully considered the entire record before us, and we will reverse the obviousness rejection of claims 1, 3, 5, 7 through 15, 23 and 25 through 28.

We agree with the examiner's findings (answer, page 7) that Ahmad discloses a process of forming a gate structure on a semiconductor substrate that includes the step of "providing a semiconductor substrate having a channel region formed therein so as to define [sic, a] source and a drain region (Ahmad fig. 5 (A), identical to steps shown in applicants' figures 1-2 etc. and described in the specification pages 4 to 6), and a gate structure comprised of a gate dielectric positioned on said channel region and a conductive layer positioned on said gate dielectric (Ahmad fig. 5(A))." We additionally agree with the examiner's finding (answer, page 7) that "Ahmad does not specifically describe implanting nitrogen in to [sic, into] said substrate." We do not, however, agree with the examiner's

finding (answer, page 7) that Ahmad conducts "source/drain reoxidation, thereby forming a sidewall spacer after implanting nitrogen . . . (Ahmad fig. 2, col. 3 Lines 53-57)."

According to the examiner (answer, page 7), "Aria in fig. 1(b), etc. and col. 12 lines 45-63 describes implanting nitrogen in to [sic, into] said substrate to better control the crystallinity thereby reducing transistor degradation and provide a transistor with better performance and reliability." Based upon the teachings of Arai, the examiner concludes (answer, page 7) that "[t]herefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Arai's implantation step in Ahmad's process to better control the crystallinity thereby reducing transistor degradation to provide a transistor with better performance and reliability . . . (Arai col. 13 lines 60-64)."

Even if we assume for the sake of argument that the skilled artisan would have found it obvious to implant nitrogen as taught by Aria into the semiconductor structure of Ahmad (Figure 4A) prior to implanting arsenic into the semiconductor substrate (Figure 5A) "to better control the crystallinity thereby reducing

transistor degradation to provide a transistor with better performance and reliability," we still must agree with the appellant's argument (brief, page 7) that "neither of the references teaches or suggests a combination of the steps or the particular sequence of the steps recited in the pending claims." Ahmad performs the source/drain reoxidation step (Figure 2; column 3, lines 53 through 57) before any implant is placed into the substrate, whereas the claims on appeal perform the source/drain reoxidation or oxidation after the nitrogen is implanted into the substrate.

In summary, the obviousness rejection of claims 1, 3, 5, 7 through 15, 23 and 25 through 28 is reversed because the combined teachings of the references neither teach nor would have suggested to one of ordinary skill in the art the specifically claimed process steps for forming a gate structure on a semiconductor substrate.

Appeal No. 2005-0426
Application No. 09/397,952

DECISION

The decision of the examiner rejecting claims 1, 3, 5, 7 through 15, 23 and 25 through 28 under 35 U.S.C. § 103(a) is reversed.

REVERSED

KENNETH W. HAIRSTON
Administrative Patent Judge

Anita Pellman Gross
ANITA PELLMAN GROSS
Administrative Patent Judge

LANCE LEONARD BARRY
Administrative Patent Judge

BOARD OF PATENT
APPEALS AND
INTERFERENCES

KWH / dpv

Appeal No. 2005-0426
Application No. 09/397,952

KNOBBE MARTENS OLSON & BEAR, LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614